

Claims

We claim:

1. A family of transistor devices formed in a semiconductor substrate, said substrate being doped with P-type impurity and not comprising an epitaxial layer, said substrate comprising an N-type isolation region extending downward from a surface of said substrate, said N-type isolation region comprising a deep N layer and an annular N well and enclosing an isolated region of said P-type substrate, said family of devices being formed in said isolated region and comprising:
 - a PNP transistor comprising:
 - 10 an implanted P well adjacent said surface of said substrate, said P well forming a collector of said transistor;
 - an N-type base region located adjacent said surface within said P well, said N-type base region forming a base of said transistor; and
 - 15 a P-type region located adjacent said surface within said N-type base region, said P-type region forming an emitter of said transistor;
 - a PMOS comprising:
 - 20 an N well having a relatively deep central portion and relatively shallow side portions, said relatively shallow side portions underlying a field oxide layer, said relatively deep central portion underlying a first opening in said field oxide layer, said N well having a breakdown voltage;
 - 25 a first gate separated from said substrate by a first gate oxide layer;
 - a P-type source region located at the surface of said substrate on one side of said first gate; and
 - 25 a P-type drain region located at the surface of said substrate on an opposite side of said first gate from said P-type source region; and
 - an NMOS comprising:
 - 30 a P well having a relatively deep central portion and relatively shallow side portions, said relatively shallow side portions underlying the field oxide layer, said relatively deep central portion underlying a second opening in said field oxide layer, said P well having said breakdown voltage;

a second gate separated from said substrate by a second gate oxide layer;

an N-type source region located at the surface of said substrate on one side of said second gate; and

5 an N-type drain region located at the surface of said substrate on an opposite side of said second gate from said N-type source region.